Notice of Allowability	Application No.	Applicant(s)	
	10/087,872	MORISHITA, YUKIKO	
	Examiner	Art Unit	
	Chuc D Tran	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *3/17/04*.

2. ☒ The allowed claim(s) is/are *1,2,4,5,7-10,12-16 and 18-21*.

3. ☒ The drawings filed on *01 February 1931* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 3/17/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Don Wong
Supervisory Patent Examiner
Technology Center 2800

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-2, 4-5, 7-10, 12-16 and 18-21 are allowed.

2. The following is an examiner's statement of reasons for allowance:

Regarding claim 1, the reference of the Prior Art of record fails to teach or suggest the combinations of the limitations as set forth in the claim: a mount member having a mount surface, wherein said semiconductor light-emitting device chip is connected to the mount surface of said mount member by solder between the semiconductor light-emitting device chip and said mount surface of said mount member, with said stack facing said mount surface, and specifically comprising the limitation of said mount member includes a material higher in thermal expansion coefficient than a material for said chip substrate.

Regarding claims 4-5, 7 and 19 are allowable for the reason given in the claim above because of their dependency status from the claim 1.

Regarding claim 2, the reference of the Prior Art of record fails to teach or suggest the combinations of the limitations as set forth in the claim: a mount member having a mount surface, wherein said semiconductor light-emitting device chip is connected to the mount surface of said mount member by solder between the semiconductor light-emitting device chip and said mount surface of said mount member, with said stack facing said mount surface, and specifically comprising the limitation of said mount surface is curved to protrude and said semiconductor light-emitting device chip is curved along and connected to said mount surface.

Regarding claims 8 and 9 are allowable for the reason given in the claim above because of their dependency status from the claim 2.

Regarding claim 10, the reference of the Prior Art of record fails to teach or suggest the combinations of the limitations as set forth in the claim: a mount member having a mount surface, wherein said semiconductor light-emitting device chip is connected to the mount surface of said mount member by solder between the semiconductor light-emitting device chip and said mount surface of said mount member, with said stack facing said mount surface, and specifically comprising the limitation of said mount member includes a material higher in thermal expansion coefficient than a material for said chip substrate.

Regarding claims 12 and 20 are allowable for the reason given in the claim above because of their dependency status from the claim 10.

Regarding claim 13, the reference of the Prior Art of record fails to teach or suggest the combinations of the limitations as set forth in the claim: a mount member having a mount surface, wherein said semiconductor light-emitting device chip is connected to the mount surface of said mount member by solder between the semiconductor light-emitting device chip and said mount surface of said mount member, with said stack facing said mount surface, and specifically comprising the limitation of said mount surface is curved to protrude and said semiconductor light-emitting device chip is curved along and connected to said mount surface.

Regarding claims 14 and 15 are allowable for the reason given in the claim above because of their dependency status from the claim 13.

Regarding claim 16, the reference of the Prior Art of record fails to teach or suggest the combinations of the limitations as set forth in the claim: a mount member having a mount surface, wherein said semiconductor light-emitting device chip is connected to the mount surface of said mount member with said stack facing said mount surface, and specifically comprising the

limitation of said mount member includes a material higher in thermal expansion coefficient than a material for said chip substrate to include said mount surface and said stack are connected by solder and said solder includes at least one selected from the group consisting of In, Sn, Pb and Au.

Regarding claims 18 and 21 are allowable for the reason given in the claim above because of their dependency status from the claim 16.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Citation of relevant Prior Art

Prior Art Karker et al (US. 2001/0038140) disclose multi-layered semiconductor package.

Prior Art Chen (USP. 6,531,328) disclose packaging of light emitting diode.

Prior Art Kamiyama et al (USP. 5,787,104) disclose semiconductor light emitting device.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuc D Tran whose telephone number is (571) 272-1829. The examiner can normally be reached on M-F Flex hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on (571) 272-1834. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TC
November 8, 2004

Don Wong
Supervisory Patent Examiner
Technology Center 2800